

WHAT IS CLAIMED IS:

1. A power semiconductor device comprising:
 - a first semiconductor layer;
 - a second semiconductor layer of a first conductivity type formed on the first semiconductor layer;
 - 5 first and second main electrodes formed on the second semiconductor layer separately from each other;
 - a control electrode formed on the second semiconductor layer between the first main electrode and the second main electrode; and
 - 10 a third semiconductor layer formed on the second semiconductor layer between the control electrode and the second main electrode.
- 15 2. The power semiconductor device according to claim 1, further comprising:
 - a fourth semiconductor layer of a second conductivity type formed on the third semiconductor layer; and
 - 20 a field plate electrode formed on the fourth semiconductor layer.
3. The power semiconductor device according to claim 2, wherein the field plate electrode is electrically connected to the first main electrode.
- 25 4. The power semiconductor device according to claim 3, wherein the third semiconductor layer has a thickness that is smaller than a distance between the

control electrode and the second main electrode.

5. The power semiconductor device according to
claim 1, further comprising a fifth semiconductor layer
of the first conductivity type formed under the second
main electrode.

6. The power semiconductor device according to
claim 5, wherein the third semiconductor layer and the
fifth semiconductor layer are arranged so as to overlap
each other in a height direction thereof.

10 7. The power semiconductor device according to
claim 6, wherein the fourth semiconductor layer and the
fifth semiconductor layer are arranged so as to overlap
each other in a height direction thereof.

15 8. The power semiconductor device according to
claim 7, wherein the third semiconductor layer has a
thickness that is smaller than a distance between the
control electrode and the fifth semiconductor layer.

9. The power semiconductor device according to
claim 3, wherein the third semiconductor layer is
20 formed so as to cover the second main electrode.

10. The power semiconductor device according to
claim 9, wherein the fourth semiconductor layer and the
second main electrode are arranged so as to overlap
each other in a height direction thereof.

25 11. The power semiconductor device according to
claim 10, wherein the third semiconductor layer has a
thickness that is smaller than a distance between the

control electrode and the second main electrode.

12. The power semiconductor device according to
claim 1, further comprising:

5 an insulation film formed on the third
semiconductor layer; and
a field plate electrode formed on the insulation
film.

10 13. The power semiconductor device according to
claim 12, wherein the field plate electrode is
connected to one of the first main electrode and the
control electrode.

14. The power semiconductor device according to
claim 3, further comprising a gate insulation film
formed under the control electrode.

15 15. The power semiconductor device according to
claim 1, wherein the first semiconductor layer and the
second semiconductor layer form a heterojunction of
AlGaN and GaN.

20 16. The power semiconductor device according to
claim 1, wherein the first semiconductor layer and the
second semiconductor layer form a heterojunction of
AlGaN and GaInN.

25 17. The power semiconductor device according to
claim 15, wherein the second semiconductor layer has
a band gap that is wider than that of the first
semiconductor layer.

18. The power semiconductor device according to

claim 16, wherein the second semiconductor layer has a band gap that is wider than that of the first semiconductor layer.

19. The power semiconductor device according to
5 claim 17, wherein the third semiconductor layer has a band gap that varies in a depth direction thereof.

20. The power semiconductor device according to
claim 18, wherein the third semiconductor layer has a band gap that varies in a depth direction thereof.

10 21. The power semiconductor device according to
claim 19, wherein the third semiconductor layer has a band gap that is wider than that of the fourth semiconductor layer.

15 22. The power semiconductor device according to
claim 20, wherein the third semiconductor layer has a band gap that is wider than that of the fourth semiconductor layer.

20 23. The power semiconductor device according to
claim 3, wherein the first, second, third and fourth semiconductor layers are each formed of diamond.

24. The power semiconductor device according to
claim 2, wherein the first, second, third and fourth semiconductor layers each have a band gap of 3 eV or more.

25 25. The power semiconductor device according to
claim 1, wherein the first and third semiconductor layers are each formed of an intrinsic semiconductor.

26. A power semiconductor device comprising:

a first semiconductor layer;

a second semiconductor layer of a first

conductivity type formed on the first semiconductor

5 layer;

an anode electrode formed on the second semiconductor layer, the anode electrode and the second semiconductor layer forming a Schottky junction;

a cathode electrode formed on the second

10 semiconductor layer and electrically connected to the second semiconductor layer; and

a third semiconductor layer formed on the second semiconductor layer between the anode electrode and the cathode electrode.

15 27. The power semiconductor device according to claim 26, further comprising:

a fourth semiconductor layer of a second conductivity type formed on the third semiconductor layer; and

20 a field plate electrode formed on the fourth semiconductor layer and electrically connected to the anode electrode.

25 28. The power semiconductor device according to claim 27, wherein the first, second, third and fourth semiconductor layers each have a band gap of 3 eV or more.

29. The power semiconductor device according to

claim 28, wherein the first and third semiconductor layers are each formed of an intrinsic semiconductor.

30. The power semiconductor device according to claim 29, wherein the first and third semiconductor layers each have an impurity concentration of
5 $1.0 \times 10^{14} \text{ cm}^{-3}$ or lower.